Prototype: Enabling Commercial Off-the-Shelf LED Bulbs With Internet Protocol Connectivity

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***Abstract*—With the commercial off-the-shelf (COTS) light emitting diode (LED) bulbs widely applied for illumination in the consuming market, this potentially pushes forward the visible light communication to promote a rapid development. It provided a promising candidate for Internet access due to its larger license-free bandwidths, a cost-optimized and hybrid Internet access scheme by augmenting the existing facilities. In this paper, a wireless Internet access prototype based on COTS LED bulb has been proposed. This system features integration with a full of TCP/IP protocol stack and software-based transceiver design, which has the advantage of cost-efficient, low-complexity, and high-flexibility.**

***Keywords*—** COTS; LED; VLC; Bulb; Illumination; PD; Beaglebone; ARM; PRU.

I. Introductions

Since the high-efficiency and high-power much higher than a conventional light source, the light emitting diode (LED) has been widely used in consumer electronics, light bulbs, cars, display screens, indicators and signs. As a result, it is possible to control light brightness at a higher frequency for illumination and communication simultaneously. This idea, called visible light communication (VLC) or light fidelity (LiFi), has been proposed in 2003 and 2011 respectively [4, 1]. As for increasing bandwidth needs for Internet access, this technique is an available mean to solve "last mile" bottleneck problem because of widely distribute existing infrastructure. However, despite over the decade of development, there is no full solution for commercial off-the-shelf (COTS) LED-based network access with low cost.

As an Internet access point using VLC technology, fig. 1 shows a framework with N hops in a star topology which has been established by the IEEE 802.15.7 VLC Task Group [5]. In this networking, the Internet access point use two or more wireless hops to stored-and-forward information with light among other LED bulbs [2]. Thus, as for seamless handover requirements in each bulb, it is critical for Internet access functions with full of protocol stack. Besides, it is very useful for research and production.

This paper describes a prototype realization of an Internet access device based on COTS LED Bulbs. The foundation is Linux network driver and a software-based firmware for specified VLC transceiver circuits. The bulbs can provide wireless Internet access and light illumination simultaneously. In the following section, we gives an insight of this prototype's details. Then, in the next section we made some tests to demonstrate the validation of this design. The paper also concludes this scheme in last section.

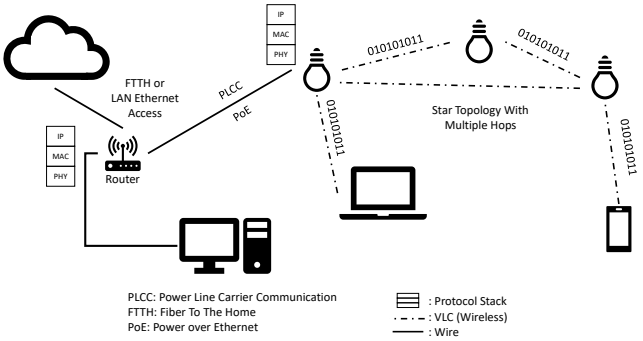

Fig. 1. The star topological structure of Internet access point using VLC technique with multiple hops

II. Platform and Architecture

The Beaglebone series of single board computer (SBC) with a TI AM335X Sitara System-On-Chip contain two programmable real-time units (PRUs). When explore the high-performance and low-power network devices, the primary 32-bit ARM processor on the AM335X can provide high compute power (1 GHz) and rich ecosystem of extensions through the Debian GNU/Linux operating system. The PRUs are intended to targeted at real-time applications where predictable response is required. Thus, the Beaglebone Black (BBB) has been employed in this scheme for protype development.

Fig. 2 shows the overall system architecture on this networked access intermediate point based on VLC. To make use of higher-level network protocols which defined by open systems interconnection (OSI) model, the media access control (MAC) layer and upper of VLC network access device is implemented by an ARM running a Linux Debian [10]. As for physical layer's (PHY's) digital part, the PRUs are fast (32 bit, 200 MHz) processor with access to a number of the general-purpose input/output (GPIO) port and internal memory and peripherals on the AM335x processor. They are capable of implementing things like pulse-width modulators, soft communication peripheral, digital codecs-machine and much more. Especially for physical layer implementation of OSI model, using the two standalone micro-controller can achieve

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low price and high performance. In short, this layer-oriented architecture is designed with the purpose of a balancing for real-time and complexity.

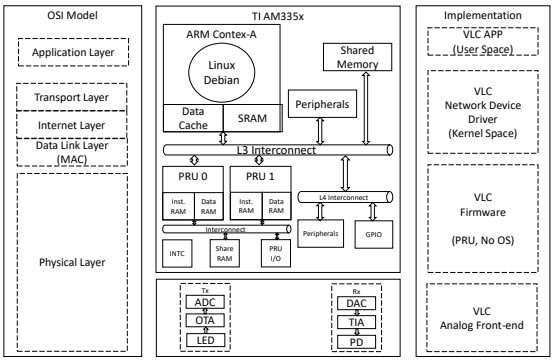

Fig. 2. The system architecture of VLC Linux network access device based on OSI layer-oriented

A. Linux-based Network Driver

Network device drivers receive and transmit data packets on hardware interface that connect to external systems and provide a uniform interface that network protocols can access. The Linux kernel has provided an implementation of TCP/IP protocol and interfaces for network devices [8]. In fact, Linux network drivers follow a fairly typical route in processing: the kernel boots up, initializes data structures, sets up some interrupt routines, and tells the network card where to put IP packets when they are received. As shown in Fig. 3, when an IP packet is actually received, the card (PRU firmware) signals the kernel causing it to do some processing and then cleans up some resources for next receive IP packet. As for transmitting IP packet from upper layers, it will be processed according to MAC frame packing rule in sequence.

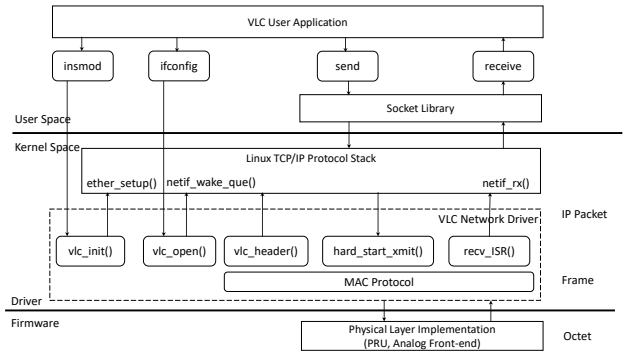

Fig. 3. The process of delivery-receiving IP packets for Linux VLC network driver

At present, No specific MAC Layer protocols for VLC are already in place. The simple Serial Line Internet Protocol (SLIP) protocol has been employed in this scheme. The MAC frame transmission with SLIP protocol composed only of data to be sent followed by an end of transmission character. The SLIP does not provide error detection, being reliant on upper layer protocols for this. It is however still useful for testing systems and easy to be substituted by another more suitable mechanism. Besides, It's low complexity and no requirement for excessive resource consumed when embedded this part into Linux driver code.

B. Software-based Baseband Controller

The physical layer of OSI model deals with bit-level transmission between different devices. There are more real-time needs when face to sampling and control tasks in PHY. Although a lot of dedicated solutions available for this, such as standalone micro-controller connected via UART [7], the additional onchip PRUs belong to the BBB's microprocessor can offer lower prices with higher integration and performance. Two build-in PRUs can be used as control unit of transmitter (Tx) and receiver (Rx) respectively. The Tx side provides programmable channel coding and modulation functions, so as to flow-controlled services. The Rx side expects that when a frame is received it is immediately extracted from the circular buffer, and notice controller of the upper layer to transfer frames from shared memory. The scheme based on build-in PRUs connected by inner bus as controller for Tx and Rx side can reduce the process delay, maximize the performance of hardware with cost-efficiency, especially for software-based modulation and data recovery technique.

1) Softwared-based Coding and Modulation: Since the non-coherent of LED bulbs used in illumination, the intensity modulation and direct detection (IM/DD) usually used in VLC systems in the optical domain. As for baseband modulation schemes, this software-based PHY controller will easily support pulse amplitude modulation (PAM), pulse position modulation (PPM), pulse interval modulation (PIM), and so on. The binary PAM, also popularly known as onoff keying (OOK), is implemented depending upon the method used to encode information into the optical carrier.

2) Data Recovery Based on Oversampling: In order to simplify the design of receiver's clock and data recovery (CDR), asynchronous serial communication (ASC) technique has been employed in this scheme. It is a form of serial communication in which the communicating endpoints' interfaces are not continuously synchronized by a common clock signal. Instead of a generic synchronization signal, the data stream contains synchronization information in form of start and stop signals, before and after each unit of transmission, respectively. The start signal prepares the receiver for arrival of data and the stop signal resets its state to enable triggering of a new sequence. The sampling theorem introduces the concept of a sample rate that is sufficient for perfect fidelity for the original signal. As show in Fig. 4, the oversampling clock recovery has been used as receive signal wave edge detection. Data is obtained by sampling data by multi-phase clock which at least three samples are needed. When transmitter rate changed, the sampling clock in receiver side must also be changed. It can take less lock time for synchronization with low complexity, although which information rate reduced by start and stop bit.

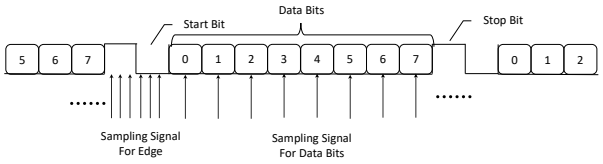

Fig. 4. A basic diagram for data recovery based on oversampling in software-based receiver

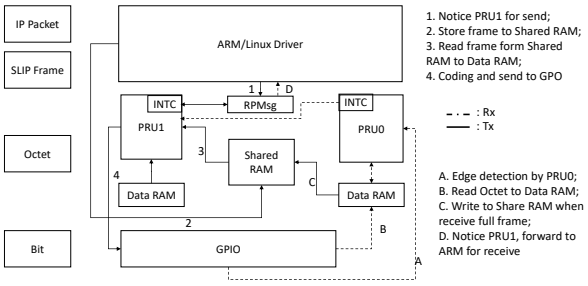

Fig. 5. RPMsg-based interruption mechinsem and nested loop FIFO for data frame transfer between ARM and PRU

3) Date Flow Between MAC and PHY: After one VLC frame is encapsulated in the MAC layer by ARM & Linux kernel driver, the PHY layer transmitter (PRU1) is required to connect the MAC layer, coding and modulate this VLC frame. Meanwhile, the other PRU need to deliver the received VLC frame to MAC layer in time. As shown in fig. 5, the data flow among multiple micro-processer is implemented by remote processor messaging (RPmsg) mechanism and data exchange in PRUs shared RAM [3]. For transmit path, the ARM write the frame to assigned RAM space at first, and then send the request information of VLC frame to PRU1 (Tx controller) by RPmsg channel at first. At last, the PRU1 will process the data with baseband mapping regulation by transmitting finite state machine (FSM) state. For receive process, because of using SLIP over ASC in this scheme, a special "End" byte distinguishes IP packet boundaries in the byte stream with a small overhead. The PRU0 (Rx controller) can easily get one complete frame and store in buffer. The PRU0 notice the PRU1 for transfer massage to ARM after receiving one VLC frame, and write this frame to shared RAM simultaneously. As a master controller, only the PRU1 construct the RPMsg channel between ARM and PRU.

In order to match the PHYs data rate with the MACs, the PHY need to buffer almost an entire maximum size frame in Tx side, and more in Rx side. Once the PHY has finished transmission and emptied its transmit buffer it can deassert carrier sense to signal it is prepared to receive another transmit frame from the MAC. To eliminate the receive frame overlay by new coming frame, a nested loop FIFO structure has been designed for solving this question.

C. Analog Front-end Circuitry

One daughter board for this prototype as an attachment to BBB has been designed. The bottom part of Fig. 2 shows the block diagram of analog front-end circuitry for VLC network access device, it can be divided into two independent circuit which is mainly for analog signal process. The following part will discuss every single block of this diagram.

1) LED Driver and Power Supply: LED lighting have a significant electrical efficiency with some chips able to emit more than 300 lumens per watt. Besides illumination, using LEDs for communication is an alternative way to ubiquitously access data and audio-video content. In order to provide enough light brightness, the socket-based LED bulb is formed by connecting multiple LED chips in series.

The AL8805 is a step-down DC/DC converter designed to drive LEDs with a constant current. The device can drive up to 8 LEDs, depending on the forward voltage of the LEDs, in series with a voltage from 6V to 36V. As shown in fig 6, series connection of LEDs provides identical LED currents resulting in uniform brightness and eliminating the need for ballast resistors. The AL8805 switches at frequency up to 1 MHz. The CTRL port can be driven by an external DC voltage to adjust output current for LED. The LED current decrease linearly with the input voltage from 0.5V to 2.5V.

$$I_{LED} = V_{CTRL} * \frac{V_{THD}}{V_{REF} * R_{SET}}, V_{CTRL} \rightarrow [0.4V, 2.5V] \quad (1)$$

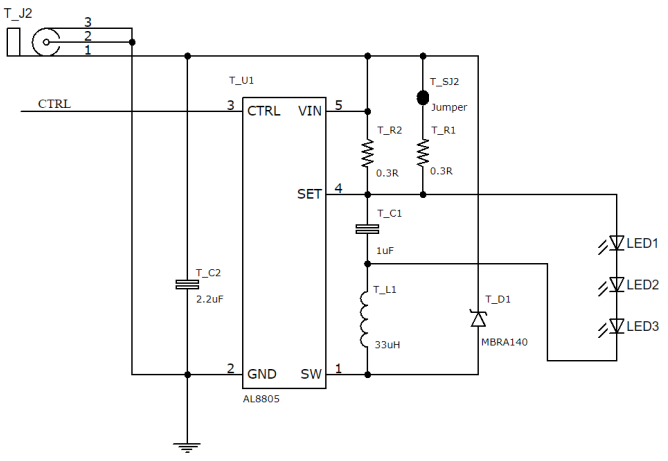

Fig. 6. A basic OTA circuits based on AL8805 for VLC transmitter amplification

LED chips can not run on the alternating current (AC) voltage directly, which require some form of driver to convert

the voltage from AC to controlled direct current (DC) for proper operation. The majority of socket-based LED lamps are self-driven in the market. In addition, an appropriate DC/DC converter is needed to power supply for the communication link and dimming control. As shown in fig. 7 The LD1085 is a low drop voltage regulator able to provide up to 3 A of output current. It can drive the BBB with a regulated 5 VDC and an additional load, up to 2.5 Amps total, from a 6 to 28 VDC supply.

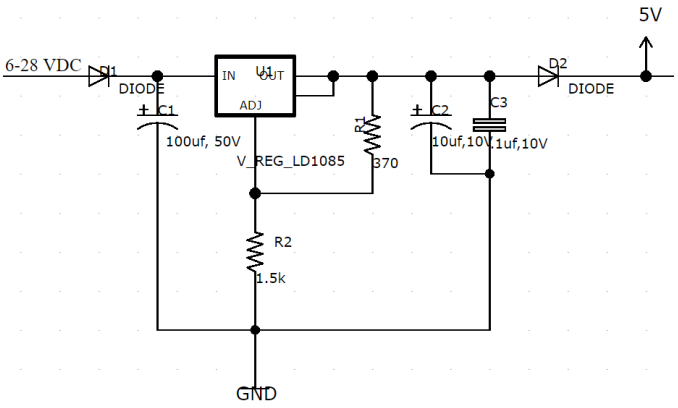

Fig. 7. A basic DC/DC circuits based on LD1085 for socket LED bulbs

2) Light Sensor and Amplification Circuit: There is a range of different types of light sensors which can use to detect the current ambient light level. Photodiode (PD) has been employed in this scheme. The more shorter response time, and the appropriate range of spectral bandwidth of PD is taken as an important index to judge it can be weather meet the VLC link rate needs or not. In addition, the parameter of PD, reverse light current, is another important parameter for the design of amplification circuits.

Fig. 8 shows the trans-impedance amplifier (TIA) circuits based on OPA320 configured to amplify the light-dependant current of PD, and drive the built-in analog-to-digital converter (ADC) of AM335x ARM microprocessor. The proper design of a single supply PD amplifier requires the consideration of many factors including stability and input and output voltage range limitations. Furthermore, the effects of input bias current and input offset voltage is often ignored and can degrade the transient response of these circuits. This design will examine the proper design process for PD amplifiers used in single supply applications. A bias voltage is applied to the op amps non-inverting input to prevent saturation at the negative power supply.

The microprocessor AM335x of BBB has a 12-bit successive approximation ADC module with a 1.8 V reference which uses successive approximation and can take 200,000 samples per second. This means the BBB can read voltage levels from 439.563 uV to 1.8 V. Therefore, The maximum output voltage should set at 1.8 V, thereby avoiding additional circuits to scale down the voltage for which sensor's pre-amplifier goes above 1.8 V. The ADC samples the received analog signal with a Nyquist rate which related to the bandwidth of transmitted

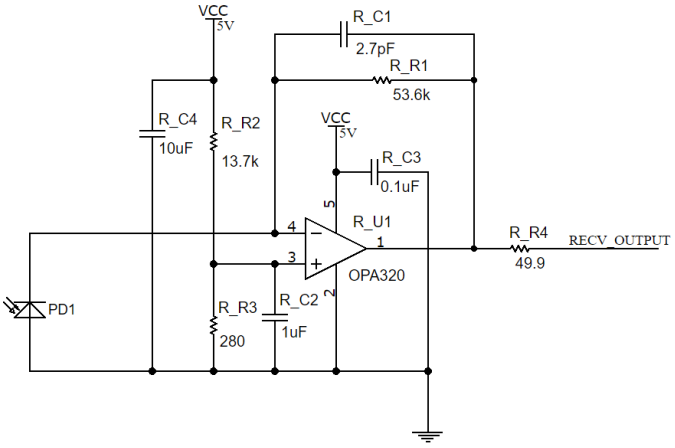

Fig. 8. A basic TIA circuits based on OPA320 for VLC receiver amplification

signal. It means that the transmit speed should less than 100 kHz in this scheme, which can really rebuild the signal without any loss.

$$V_{OUTPUT} = i_{PD} * R_1 + V_{CC} * \frac{R_3}{R_2 + R_3} \rightarrow [439.5uV, 1.8V] \quad (2)$$

III. Operation and Validation

To demonstrate that the modified light bulb is in a position to emit light with an encapsulated signal, the following measurements are reported. To show the modulated light, a PD is connected to an oscilloscope to measure the light intensity over time. Fig. 9 shows the setup for validation of this prototype.

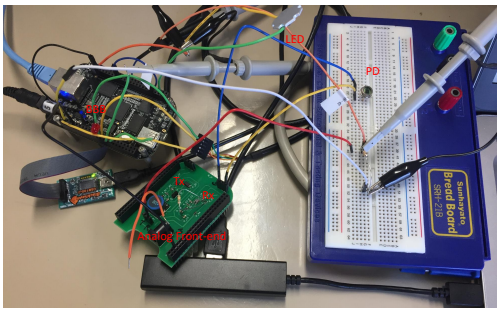

Fig. 9. The experiment setup based on single RGB-LED and PIN-PD for test prototype

A. Evaluation for Analog Front-end Circuits

There are many factors can affect the maximum rate that this prototype can reach, such as the LED's response time, PD's rise and fall time, TIA's frequency response range, so as to modulation and coding method. Use the BBB output a pulse from 1 Hz to 1 MHz which can drive the LED bulbs for illumination. As shown in Fig. 10, the eyes of human can not

perceptible for flicker when frequency is more than 73 Hz. When the frequency is more than 100 kHz, the signal gets a distortion with a large extent which can hardly recover the signal.

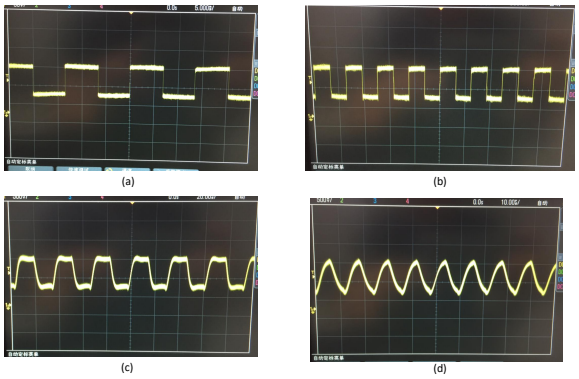

Fig. 10. The receiver signal wave after the TIA circuit by the different transmit frequency. (a) 73 Hz; (b) 1 kHz; (c) 33 kHz; (d) 100 kHz

B. Connectivity Test with Loop-back Mode

When test the link connectivity, we should start firmware in the PRUs at first. Then the Tx and Rx FSM will go into 'IDLE' state. The Tx side waits the RPMsg from ARM to transfer the MAC frame, and the Rx side oversampling the input port's signal for start edge detection. In the following step, the ARM/Linux network device driver set up the point-to-point link with IP protocol in the network layer. After the registration and initiation function, one IP packet can be sent in the loop-back mode for testing the connectivity between Tx and Rx side.

SendIP is a tool which allows creating and sending arbitrary IP packets. A wide variety of header types are supported and allow detailed control of all header fields. Therefore, it can be used to test the connectivity for this loop-back VLC link. As shown in Fig. 11, we can found that when wen send test characters "0xcafe", then the Rx function can decode the information rightly.

Fig. 11. The procedure of connectivity test with loop-back mode

IV. Conclusions

In this paper, we proposed a cost-efficient and low-complexity prototype for VLC communication using COTS LED. It aims at an Internet access with fully protocol stack. Compared with the other scheme, such as OpenVLC [9], it has better potential performance improvement in the same platform based on maximizing the efficiency of hardware investment. Sine the partial physical layer implementation of OpenVLC run in Linux driver, the key for a maximum transmission rate of this scheme is the read speed from the ADC's samples. However, the Debian distribution of Linux, which employed by OpenVLC, is not a real-time system. The move toward increased transmission rates should be limited by the low accuracy of the timing system in this non-real-time operate system.

In OSI Model, The physical layer deals with bit-level transmission between different devices and supports electrical interfaces being connected to the physical medium for synchronized communication. Thus, it has high requirements for the real time performance than other network layers. Instead, the flexibility is an important factor when a number of interconnected devices MAC and above layers. The Disney research has proposed a low rate VLC scheme which also used COTS LED bulbs for transmitter [6]. In this scheme, one microprocessor is extended with a system on chip (SoC) running a Linux distribution for MAC and above. The other micro-controller running the VLC firmware is connected via the UART interface to the SoC. Thus, the low speed UART interface can become a possible bottleneck for this scheme.

As for this scheme, it has the advantage of cost-efficient, low-complexity and high-flexibility. But besides that, there are certain defects in this prototype scheme. Although ASC method can reduce the complexity for CDR circuits and no requirement for continuously synchronized by a common clock signal, the information rate no doubt is reduced by synchronous bit, too. Therefore, the software-based CDR is great challenge for improving the information speed. But fortunately, it is not difficult to extend and update based on software transceiver structure.

Acknowledgment

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